| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/766,410 | LEE, CHEON-SU | |
| | Examiner | Art Unit | |
| | Christopher A. Daley | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--*

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/03/2006*.

2. ☒ The allowed claim(s) is/are *1-17*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

## DETAILED ACTION

### *Allowable Subject Matter*

1. The following is an examiner's statement of reasons for allowance: Independent claim 1 is allowable over the prior art of record because the examiner found neither prior art cited in its entirety, nor based on the prior art found any motivation to combine any of said prior art. The following limitations were not found in the prior art of record: Storing a first bus occupancy rate for each of the CPU and the second and third master devices and a variable bus occupancy rate; Applying a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU, and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices to a bus arbiter, in response to an activation of an interrupt signal provided to the CPU; Applying a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first bus occupancy rates for the second and third master devices to the bus arbiter, in response to an inactivation of the interrupt signal; and controlling a priority for use of the system bus in accordance with the second and third bus occupancy rates for the CPU and the first bus occupancy rates for the second and third master devices that are applied to the bus arbiter.

Independent claim 2 is allowable over the prior art of record because the examiner found neither prior art cited in its entirety, nor based on the prior art found any motivation to combine any of said prior art. The following limitations were not found in the prior art of record: Storing a first bus occupancy rate for each of the CPU and the

second and third master devices and a variable bus occupancy rate; Applying a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU, and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices to a bus arbiter, in response to an activation of a privilege mode signal provided by the CPU; Applying a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first bus occupancy rates for the second and third master devices to the bus arbiter, in response to an inactivation of the privilege mode signal; and controlling a priority for use of the system bus in accordance with the second and third bus occupancy rates for the CPU and the first bus occupancy rates for the second and third master devices that are applied to the bus arbiter.

Independent claim 3 is allowable over the prior art of record because the examiner found neither prior art cited in its entirety, nor based on the prior art found any motivation to combine any of said prior art. The following limitations were not found in the prior art of record: Storing a first bus occupancy rate for each of the CPU and the second and third master devices and a variable bus occupancy rate; Applying a second bus occupancy rate for the CPU, which is a sum of the first bus occupancy rate for the CPU, and the variable bus occupancy rate, and the first bus occupancy rates for the second and third master devices to a bus arbiter, in response to an activation of an interrupt signal provided to the CPU or a privilege mode signal provided by the CPU ;Applying a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, and the first

bus occupancy rates for the second and third master devices to the bus arbiter, in response to an inactivation of the interrupt signal or a privilege mode signal; and controlling a priority for use of the system bus in accordance with the second and third bus occupancy rates for the CPU and the first bus occupancy rates for the second and third master devices that are applied to the bus arbiter.

Independent claim 4 is allowable over the prior art of record because the examiner found neither prior art cited in its entirety, nor based on the prior art found any motivation to combine any of said prior art. The following limitations were not found in the prior art of record: a bus arbiter receiving either a second bus occupancy rate for the CPU, which is the sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to an interrupt signal provided to the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

Dependent claim 5 is allowed as associated independent claim 4 is allowed.

Independent claim 6 is allowable over the prior art of record because the examiner found neither prior art cited in its entirety, nor based on the prior art found any motivation to combine any of said prior art. The following limitations were not found in the prior art of record: a bus arbiter receiving either a second bus occupancy rate for the CPU, which is the sum of the first bus occupancy rate for the CPU and the variable bus

occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to a privilege mode signal provided to the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

Dependent claim 7 is allowed as associated independent claim 6 is allowed.

Independent claim 8 is allowable over the prior art of record because the examiner found neither prior art cited in its entirety, nor based on the prior art found any motivation to combine any of said prior art. The following limitations were not found in the prior art of record: a device storing first bus occupancy rates for a second and third master devices and a variable bus occupancy rate for increasing or decreasing a first bus occupancy rate for the CPU: and a bus arbiter receiving either a second bus occupancy rate for the CPU, which is the sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to an interrupt signal provided by the CPU or a privilege mode signal provided by the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

Dependent claims 9 and 10 are allowed as associated independent claim 8 is allowed.

Independent claim 11 is allowable over the prior art of record because the examiner found neither prior art cited in its entirety, nor based on the prior art found any motivation to combine any of said prior art. The following limitations were not found in the prior art of record: a device storing first bus occupancy rates for a second and third master devices and a variable bus occupancy rate for increasing or decreasing a first bus occupancy rate for the CPU: and a bus arbiter receiving either a second bus occupancy rate for the CPU, which is the sum of the first bus occupancy rate for the CPU and the variable bus occupancy rate, or a third bus occupancy rate for the CPU, which is obtained by subtracting the variable bus occupancy rate from the first bus occupancy rate for the CPU, in response to an interrupt signal provided by the CPU or a privilege mode signal provided by the CPU, receiving the first bus occupancy rates for the second and third master devices, and controlling a priority for use of the system bus in accordance with received bus occupancy rates for the CPU and the second and third master devices.

Dependent claims 12 and 13 are allowed as associated independent claim 11 is allowed.

Independent claims 14 and 17 is allowable over the prior art of record because the examiner found neither prior art cited in its entirety, nor based on the prior art found any motivation to combine any of said prior art. The following limitations were not found in the prior art of record: a device storing bus occupancy rates for a plurality of cards

inserted into the respective slots and a variable bus occupancy rate for increasing or decreasing the bus occupancy rates; and a bus arbiter controlling a priority for use of the PCI bus in accordance with the bus occupancy rates for the cards in response to interrupt signals generated by the cards.

Dependent claims 15 and 16 are allowed as associated independent claim 14 is allowed.

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Cottingham can be reached on 571 272 7079. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAD
3/22/06

JOHN R. COTTINGHAM
PRIMARY EXAMINER